

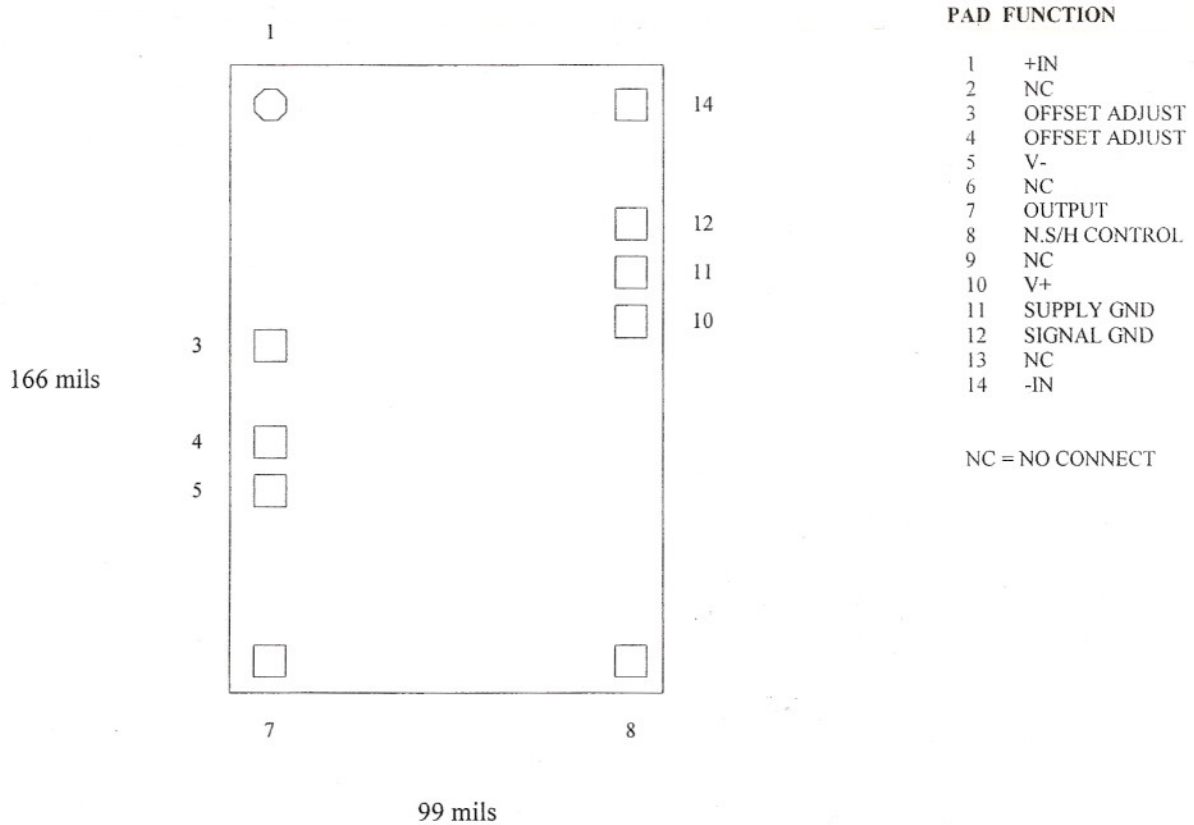


# Sierra Components, Inc.

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Chip back potential is the level which bulk silicon is maintained by on-chip connection, or it is the level to which the chip back must be connected when specifically stated below. If no potential is given the chip back should be isolated.



NOTE: Chip back must be connected to SIGNAL GND.

**Topside Metal: Al**  
**Backside: Si**  
**Backside Potential: see above**  
**Mask Ref: 3906**  
**Bond Pads: .004" min.**

**APPROVED BY: CD**

**MFG: Harris**

**DIE SIZE: .099" x .166"**

**THICKNESS: .020"**

**DATE: 7/26/02**

**P/N: HA-5330-6/2**